What is claimed is:

1. A method for timing memory access in a clocked circuit, comprising:

receiving a clock pulse used as a first strobe signal to a first strobe input of a memory for initiating a first memory access;

receiving a strobe ready signal from the memory after the first memory access;

generating a second strobe signal in response to the strobe ready signal; and

transmitting the second strobe signal to a second strobe input of the memory for initiating a second memory access during the clock pulse.

2. The method of claim 1, further comprising:

generating a select signal in response to the clock pulse; and

providing the select signal to at least one data addressing multiplexer for selecting an input for the second memory access.

3. The method of claim 1, further comprising:

providing a constant input to at least one memory select (MS) input of the memory for allowing the first memory access and the second memory access.

4. The method of claim 1, further comprising:

providing a constant signal to a first memory select (MS) input of the memory for allowing the first memory access.

5. The method of claim 4, further comprising:

generating a select signal in response to the clock pulse; and

providing the select signal to a second MS input of the memory and a data addressing multiplexer for allowing the second memory access.

6. The method of claim 1, further comprising:

generating a select signal in response to the clock pulse; and

generating the second strobe signal in response to the SR signal and the select signal.

7. The method of claim 1, further comprising:

generating the select signal from an output of a first flip-flop; and

generating the second strobe signal from an output of a second flip-flop

8. The method of claim 1, the SR signal being generated by the memory after the first memory access is complete.

9. The method of claim 1, the clock pulse comprising a clock pulse from a system clock.

10. The method of claim 1, the clock pulse comprising a positive clock pulse.

11. An apparatus for timing memory accesses, comprising:

a first flip-flop and a second flip-flop, each having a clock input, a data input and a data output;

the clock input of the first flip-flop for receiving a clock pulse from a system clock, the clock pulse for initiating a first memory access in a memory;

the data output of the first flip-flop for transmitting a select signal in response to the clock pulse, the data output of the first flip-flop further connected to the data input of the second flip-flop for receiving the select signal;

the clock input of the second flip-flop for receiving a strobe ready signal from the memory after the first memory access; and

the data output of the second flip-flop for transmitting a strobe signal to initiate a second data access for the memory during the clock pulse in conjunction with the select signal.

12. The apparatus of claim 11, the data input of the first flip-flop receiving a constant signal.

13. The apparatus of claim 11, the first flip-flop and the second flip-flop each further comprising a clear input for clearing the data output, the apparatus further comprising:

an inverter and a buffer, each having an input and an output;

the input of the inverter connected to the data output of the second flip-flop for receiving the strobe signal;

the output of the inverter connected to the clear input of the first flip-flop for transmitting a clear signal generated by inverting the strobe signal, the output of the inverter further connected to the input of the buffer for receiving the clear signal;

the output of the buffer connected to the clear input of the second flip-flop for transmitting the clear signal after a delay.

14. The apparatus of claim 11, further comprising the memory.

15. The apparatus of claim 14, the memory comprising:

a first strobe input for receiving the clock pulse and initiating the first data access in response to the clock pulse;

a second strobe input for receiving the strobe signal and initiating the second data access in response to the strobe signal and the select signal during the clock pulse.

16. The apparatus of claim 14, the memory comprising:

a strobe ready output connected to the clock input of the second flip-flop for transmitting the strobe ready signal after a completion of the first memory access.

17. The apparatus of claim 14, further comprising:

a first memory select input for receiving a first memory select signal that enables the first memory access in conjunction with the clock pulse; and

a second memory select input for receiving a second memory select signal that enables the second memory access in conjunction with the strobe signal and the select signal.

18. The apparatus of claim 17, the first memory select signal and the second memory select signal both being constant.

19. The apparatus of claim 17, the first memory select signal being constant;

the second strobe input connected to the strobe ready output for receiving the strobe ready signal; and

the second memory select input connected to the data output of the first flip-flop for receiving the select signal.

20. The apparatus of claim 14, the memory further comprising:

a data input port for receiving data and an address input port for receiving an address in the memory to provide the data, the apparatus further comprising:

a multiplexer for transmitting the data to at least one of the data input port and the address input port, the multiplexer having a select input connected to the data output of the first flip-flop for receiving the select signal, the select signal allowing a selection of the data to be provided to the memory by the multiplexer, based on a state of the select signal.